CS315-02 RISC-V Emu Imm JAL Mem

Lab 06 due Wed Oct 1 11:59 pm

Extra OH today 4:30pm to 5:30 pm

Project 04 published due Oct 7 11:59

Project 04 IG wed oct 8

Lab 07 Exam-like problems Oct 6 Mon

I will provide the Fall 2024 CS315 Midterm

Midterm Thu Oct 9

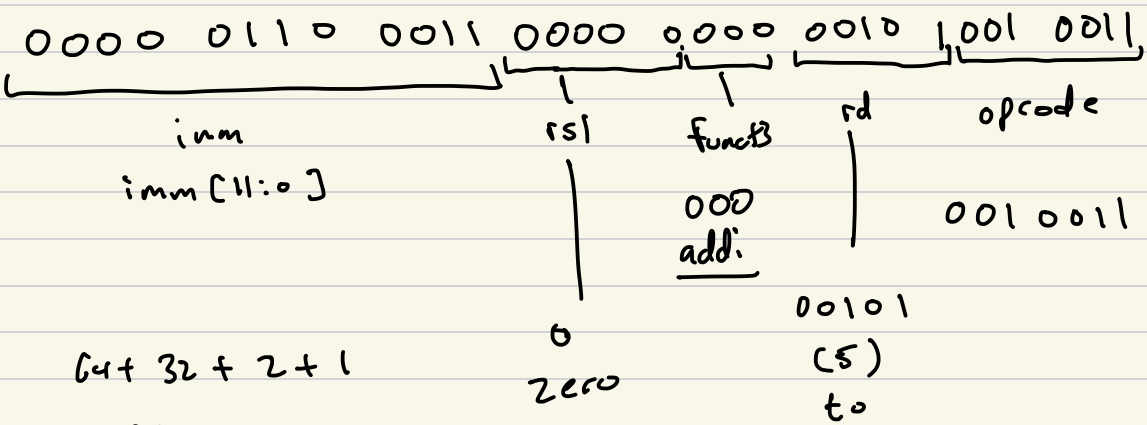
Lab 06

starter	rv_emu.c	131	LOC
solution	rv_emu.c	225	LOC

Immediate

li t0, 99 ⇒ addi t0, zero, 99

0x06300293



64 + 32 + 2 + 1

96 + 3

= 99

get_rd(iw)
get_rs1(iw)
get_funct3(iw)

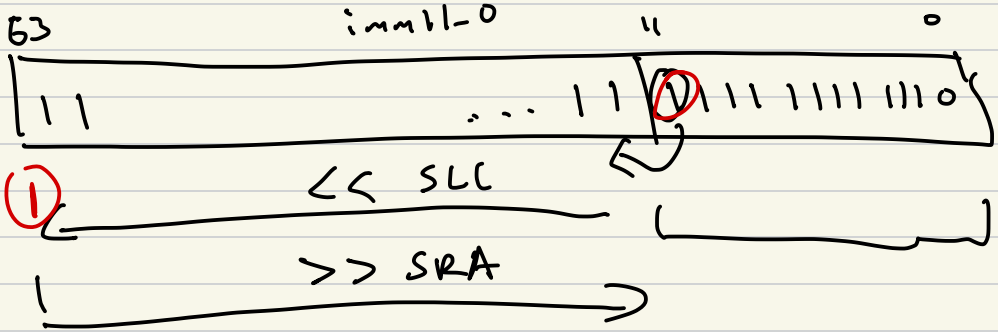
uint64_t imm11_0 = get_bits(iw, 20, 12);

li t0, -2 → addi t0, zero, -2

0xFFE0 0293

```
 1111 1111 1110
inv 0000 0000 0001
+                1
-------------------
 0000 0000 0010 (2)
```

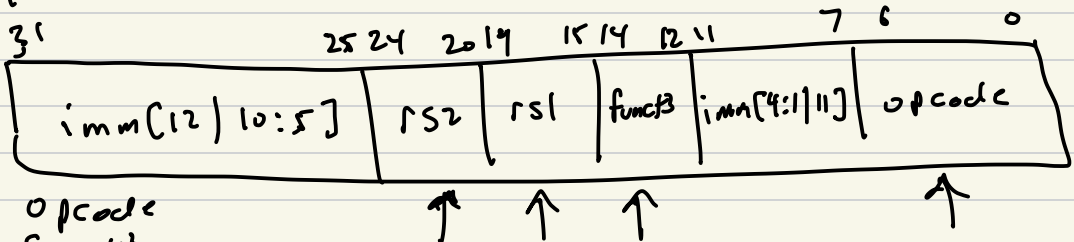
```
int64_t imm = sign_extend(imm11_0, 11)
```



Branches (B-Type)

Compare two reg values
Possibly branch to target label

Fields



opcode
funct3
rs1
rs2

imm[12] imm[11] imm[10:5] imm[4:1] 0

1) get parts

```
uint32_t imm12 = get_bits(iw, 31, 1)
uint32_t imm10_5 = get_bits(iw, 25, 6)
uint32_t imm4_1 = get_bits(iw, 8, 4)
uint32_t imm11 = get_bits(iw, 7, 1)
```

2) combine parts

```
uint64_t uimm;
uimm = (imm12 << 12) | (imm11 << 11)
     | (imm10_5 << 5) | (imm4_1 << 1) | 0
```

3) int64_t imm;

```
imm = sign_extend(uimm, 12);
```

4) Branch Logic

If you take the branch

pc = pc + imm

else

pc = pc + 4

5) Branch Condition

```
if (funct3 == 0b000) {
    if (rsp->regs[rs1] == rsp->regs[rs2]) {
        take = true;
    }
} else if (funct3 ... )
```

```
bool take
take = rsp->regs[rs1] == rsp->regs[rs2]
```

```
if (take) {
    pc = pc + imm
} else {
    pc = pc + 4
```

↑

```
rsp->pc = rsp->pc + 4;
```

JAL Jump and Link (call, j)

call → jal jal ra, imm (offset)

j → jal jal zero, imm (offset)

Memory Instructions Loads & Stores

i-type

lw to, offset(a0) lw to, 8(a0)

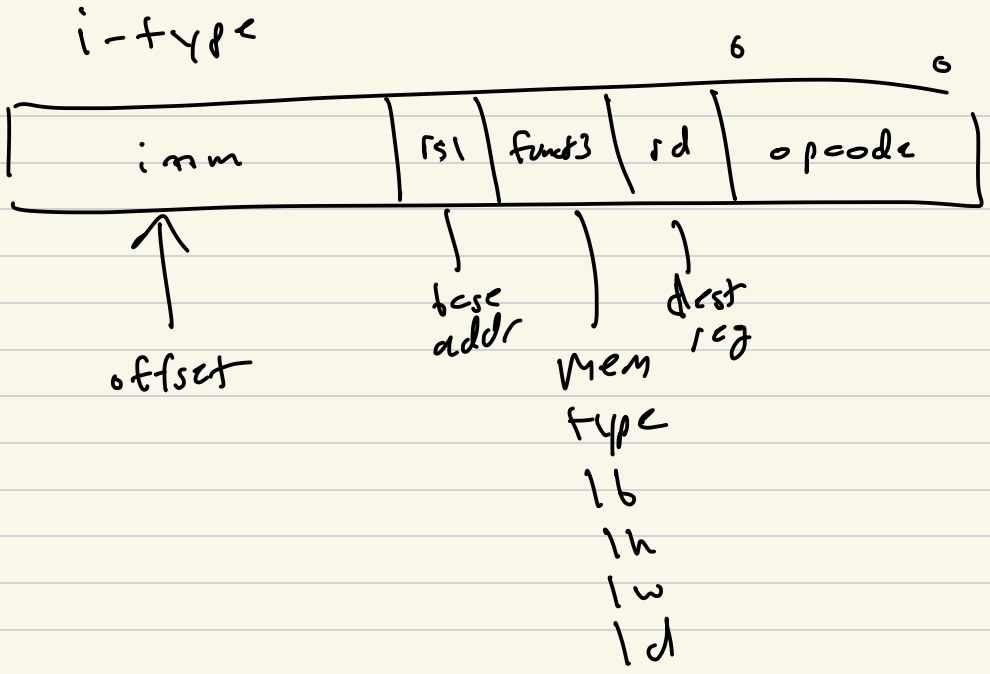
32 bit target address

to = *(a0 + offset)

Target address

TA = rs1 + imm

rd = *((uint32_t *) TA);



lb - uint8_t *
lw - uint32_t *
ld - uint64_t *

---

stores → S-Type

sw t0, 8(a0)
(rs2)

TA = rs1 + imm

sw

*((uint32_t *) TA) = regs[rs2]